Code No: R059210504 **Set No. 1**

II B.Tech I Semester Regular Examinations, November 2007
DIGITAL LOGIC DESIGN
(Common to Computer Science & Engineering, Information Technology and Computer Science & Systems Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Perform subtraction with the following unsigned decimal numbers by taking 10's complement of the subtrahend. Verify the result. [3+3+3+3]
   i. 5250 - 1321
   ii. 1753 - 8640
   iii. 20 - 100
   iv. 1200 - 250
   (b) Convert the given gray code number to equivalent binary 1001001011110010 [4]

2. (a) Draw the logic diagram corresponding to following expressions without simplifying them.
   i. (A + B) (C + D) (A' + B + D)
   ii. (AB + A'B')(CD' + C'D)
   (b) Obtain the complement of the following Boolean expressions. [8+8]
   i. x'yz + x'yz' + xy'z' + xy'z
   ii. x'yz + xy'z' + xyz + xyz'
   iii. x'z + x'y + xy'z + yz
   iv. x'y?z' + x'yz' + xy'z' + xy'z + xyz'.

3. (a) Show that $A \oplus B = (A + B) + \left(\overline{A} + \overline{B}\right)$ and draw the circuit implementation two-level NOR-NOR form and NAND-AND form.
   (b) Obtain minimal POS expression for the given Boolean function $f(A, B, C, D) = \sum 0, 1, 2, 3, 4, 8, 9, 12$ And draw the circuits with two ?level NOR-NOR form and AND- OR form. [8+8]

4. (a) Implement 64 × 1 multiplexer with four 16 × 1 and one 4 ×1 multiplexer. (Use only block diagram).
   (b) A combinational logic circuit is defined by the following Boolean functions.
   $F_1 = \overline{ABC} + AC$
   $F_2 = A\overline{BC} + \overline{A}B$
   $F_3 = A\overline{B}C + AB$
   Design the circuit with a decoder and external gates. [8+8]

5. (a) Draw the circuit diagram of clocked D- flip-flop with NAND gates and explain its operation using truth table. Give its timing diagram.

(b) Explain the procedure for the design of sequential circuits with example. [8+8]

6. (a) Write the HDL structural description of the 4- bit binary counter with parallel load.

   (b) Design a 4-bit ring counter using D- flip flops and draw the circuit diagram and timing diagrams. [8+8]

7. Tabulate the PLA programming table for the four Boolean functions:
   A(x,y,z) = Σ (1,2,4,6)
   B(x,y,z) = Σ (0,1,6,7)
   C(x,y,z) = Σ (2,6)
   D(x,y,z) = Σ (1,2,3,5,7)
   Minimize the number of product terms and also show the internal logic in the PLA structure. [16]

8. (a) Give the implementation procedure for a SR Latch using NOR gates.

   (b) An asynchronous sequential circuit is described by the excitation and output functions.
   Y = $x_1x_2' + (x_1 + x_2')$y
   Z = y
   Implement the circuit defined above with a NOR SR latch. Repeat with a NAND SR latch. [6+10]

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Code No: R059210504 **Set No. 2**

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Time: 3 hours **Max Marks: 80**

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1. (a) Perform the following using BCD arithmetic. [4+4]
   i. $7129_{10} + 7711_{10}$
   ii. $8124_{10} + 8127_{10}$
   (b) Convert the following:
   i. $AB_{16} = (\quad)_{10}$
   ii. $1234_8 = (\quad)_{10}$
   iii. $10110011_2 = (\quad)_{10}$
   iv. $772_{10} = (\quad)_{16}$ [2+2+2+2]

2. (a) Simplify the following Boolean functions.
   i. x"yz + x'yz' + xy'z' + xy'z
   ii. x'yz + xy'z' + xyz + xyz'
   iii. x'z + x'y + xy'z + yz
   iv. x'y'z' + x'yz' + xy'z' + xy'z + xyz'.
   (b) Obtain the complement of the following Boolean expressions. [8+8]
   i. A'C' + ABC + AC'
   ii. (x'y' + z)' + z + xy + wz
   iii. A'B(D' + C'D) + B(A +A'CD)
   iv. (A' + C)(A' + C')(A + B + C'D).

3. (a) Implement the following Boolean function F using no more than two NOR - gates and draw the circuit.
   $F(A, B, C, D) = \sum(0, 1, 2, 9, 11) + d(8, 10, 14, 15)$
   (b) Implement the following Boolean function using two - level forms: [6+10]
   i. NAND - AND
   ii. AND - NOR
   iii. OR - NAND and
   iv. NOR - OR and draw the circuits.
   $F(A, B, C, D) = \Pi 5, 7, 9, 11, 12, 13, 14, 15$

4. (a) Using K-map design a combinational logic circuit to obtain 2's complement for the given 4-bit binary number. Draw the circuit using only two input exclusive-OR gates and 2- input OR gates. What is the output expression for 5 inputs?

(b) Design a combinational circuit to increment a 4-bit binary number A_3, A_2, A_1, A_0 by 1 using four half - adders. [8+8]

5. Obtain state table and state diagram for sequence recognizer to recognize the occurrence of the sequence bits 1101, and design the logic circuit. [16]

6. (a) Draw the logic diagram for a 4-bit binary ripple down counter using positive edge triggered flip-flops.

   (b) Write the HDL behavioral description of the 4- bit universal shift register. [8+8]

7. List the PLA programming table and draw the PLA structure for the BCD-to-excess-3-code converter. [16]

8. (a) Give the implementation procedure for a SR Latch using NOR gates.

   (b) An asynchronous sequential circuit is described by the excitation and output functions.
   Y = $x_1x_2' + (x_1 + x_2')$y
   Z = y
   Implement the circuit defined above with a NOR SR latch. Repeat with a NAND SR latch. [6+10]

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Code No: R059210504 **Set No. 3**

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Time: 3 hours **Max Marks: 80**

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1. Convert the following to Decimal and then to Hexadecimal.
   (a) 765_8
   (b) 1002_8
   (c) 11001001_2
   (d) 11110000_2
   (e) 257_{10}
   (f) 239_{10} [3+3+3+3+2+2]

2. (a) Express the following functions in sum of minterms and product of maxterms.
      i. F (A,B,C,D) = B'D + A'D + BD
      ii. F(x,y,z) = (xy + z)(xz + y).
   (b) Obtain the complement of the following Boolean expressions. [8+8]
      i. (AB' + AC')(BC + BC')(ABC)
      ii. AB'C + A'BC + ABC
      iii. (ABC)'(A + B + C)'
      iv. A + B'C (A + B + C').

3. (a) Implement $F = (\overline{x}y + x\overline{y})\,(w + \overline{z})$ using multilevel NOR gates and draw the circuit.
   (b) Implement the following Boolean functions using wired - logic: [8+8]
   $F_1 = \overline{AB} \bullet \overline{CD}$ *use AOI gate*
   $F_2 = \overline{A + B} \bullet \overline{C + D}$ *use AOI gate*
   And draw the circuit.

4. (a) Implement 64 × 1 multiplexer with four 16 × 1 and one 4 ×1 multiplexer. (Use only block diagram).
   (b) A combinational logic circuit is defined by the following Boolean functions.
   $F_1 = \overline{ABC} + AC$
   $F_2 = A\overline{BC} + \overline{A}AB$
   $F_3 = A\overline{B}C + AB$
   Design the circuit with a decoder and external gates. [8+8]

5. (a) Convert the following

i. J-K flip-flop to T- flip-flop
ii. R-S flip-flop to D-flip-flop.

(b) Draw the circuit diagram of positive edge triggered J-K flip-flop with NAND gates and explain its operation using truth table. How race around condition is eliminated. [8+8]

6. (a) Draw and explain 4-bit universal shift register.
   (b) Explain different types of shift registers. [8+8]

7. (a) Draw and explain the block diagram of PLA.
   (b) Tabulate the PLA programmable table for the four Boolean functions given below:
   A(x,y,z) = Σ m (1,2,4,6)
   B(x,y,z) = Σ m (0,1,6,7)
   C(x,y,z) = Σ m (2,6)
   D(x,y,z) = Σ m (1,2,3,5,7). [16]

8. (a) Give the implementation procedure for a SR Latch using NOR gates.
   (b) An asynchronous sequential circuit is described by the excitation and output functions.
   Y = $x_1x_2' + (x_1 + x_2')$y
   Z = y
   Implement the circuit defined above with a NOR SR latch. Repeat with a NAND SR latch. [6+10]

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Code No: R059210504 **Set No. 4**

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Time: 3 hours **Max Marks: 80**

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1. Convert the following to Binary and then to gray code. [2+2+2+2+4+4]
   (a) 1010_{16}
   (b) $AB33_{16}$
   (c) 3323_8
   (d) 1764_8
   (e) 187_{10}
   (f) 2266_{10}.

2. (a) Convert the following expressions in to sum of products and product of sums.
      i. (AB + C) (B + C'D)
      ii. x' + x(x + y')(y + z').
   (b) Obtain the Dual of the following Boolean expressions. [8+8]
      i. (AB' + AC')(BC + BC')(ABC)
      ii. AB'C + A'BC + ABC
      iii. (ABC)'(A + B + C)'
      iv. A + B'C (A + B + C').

3. (a) If
   $F_1(A, B, C) = A \oplus B \oplus C$
   $F_2(A, B, C) = A \oplus C \oplus B$
   Show that $= F_1 = F_2$
   (b) Show that $A \oplus B \oplus AB = A + B$
   (c) Obtain minimal SOP expression for the complement of the given expression: $F(A, B, C) = \prod(1, 2, 5, 7)$ And draw the circuit using NOR - gates. [4+4+8]

4. (a) Implement 64 × 1 multiplexer with four 16 × 1 and one 4 ×1 multiplexer. (Use only block diagram).
   (b) A combinational logic circuit is defined by the following Boolean functions.
   $F_1 = \overline{ABC} + AC$
   $F_2 = A\overline{BC} + \overline{A}B$
   $F_3 = A\overline{B}C + AB$
   Design the circuit with a decoder and external gates. [8+8]

5. (a) Draw the circuit diagram of clocked D- flip-flop with NAND gates and explain its operation using truth table. Give its timing diagram.
   (b) Explain the procedure for the design of sequential circuits with example. [8+8]

6. (a) Explain synchronous and ripple counters. Compare their merits and demerits.
   (b) Design a modulo -12 up synchronous counter using T- flip flops and draw the circuit diagram. [8+8]

7. (a) Show the memory cycle timing waveforms for the write and read operations. Assume a CPU clock of 50 MHz and a memory cycle time of 50 ns.
   (b) The following memory units are specified by the number of words times the number of bits per word. How many address lines and input-output data lines are needed in each case? [8+8]
      i. 4K * 16,
      ii. 2G * 8 ,
      iii. 16M * 32,
      iv. 256K * 64.

8. (a) Describe the operation of the SR Latch using NAND gate with the help of truth table, transition table and the circuit.
   (b) Explain the operation and use of De bounce circuit. [8+8]

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