Code No: R059210505 **Set No. 1**

II B.Tech I Semester Regular Examinations, November 2007
COMPUTER ORGANIZATION
(Common to Computer Science & Engineering, Information Technology and Computer Science & Systems Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Explain the terms computer architecture, computer organization and computer design in a detailed fashion. [8]
   (b) Explain about MIPS, FLOPS rating of a processor. How do we arrive at these values. [8]
2. (a) Design a circuit transferring data from a 4bit register which uses D flip-flops to another register which employs RS flip-flops. [8]
   (b) What are register transfer logic languages? Explain few RTL statement for branching with their actual functioning. [8]
3. (a) Give the typical horizontal and vertical microinstruction formats. [8]
   (b) Describe how microinstructions are arranged in control memory and how they are interpreted. [8]
4. (a) How many bits are needed to store the result addition, subtraction, multiplication and division of two n-bit unsigned numbers. Prove. [8]
   (b) What is overflow and underflow? What is the reason? If the computer is considered as infinite system do we still have these problems. [8]
5. (a) What is a virtual memory technique? Explain different virtual memory techniques. [8]
   (b) Explain how the technique of paging can be implemented [8]
6. Explain the following:
   (a) CPU - I O P Communication
   (b) I O P
   (c) IBM 370 I/O Channel. [5+5+6]
7. Explain three segment instruction pipeline. Show the timing diagram and show the timing diagram with data conflict. [16]
8. What are the different kinds of Multi stage Switching networks? Explain with neat sketch. Compare their functioning. [16]

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Code No: R059210505 **Set No. 2**

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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Explain about sign magnitude and 2's complement approaches for representing the fixed point numbers. Why 2's complement is preferable.
   (b) Give means to identify whether or not an overflow has occurred in 2s complement addition or subtraction operations. Take one example for each possible situation and explain. Assume 4 bit registers.
   (c) Distinguish between tightly coupled microprocessors and tightly coupled Microprocessors. [16]

2. Explain about instruction, fetch, and decode cycles for a memory reference instruction. Draw a flow chart also to explain the same. Indicate clearly where and which processor registers comes into picture. Now let us assume while a instruction is in the middle of its decode cycle a interrupt is arrived. What is going to happen? Is the instruction is completed or not. If we want to stop there itself and handle the interrupt what are the difficulties? [16]

3. (a) What are the major design considerations in microinstruction sequencing? [8]
   (b) Explain about microinstruction sequencing techniques, specifically variable format address microinstruction. [8]

4. (a) How many bits are needed to store the result addition, subtraction, multiplication and division of two n-bit unsigned numbers. Prove. [8]
   (b) What is overflow and underflow? What is the reason? If the computer is considered as infinite system do we still have these problems. [8]

5. (a) A computer uses RAM chips of 1024 x 1 capacity. [10]
      i. How many chips are needed and how should their address lines be connected to provide a memory capacity of 1024 bytes.
      ii. How many chips are needed to provide a memory capacity of 16K bytes.
   (b) An address space is specified by 24 bits and the corresponding memory space by 16 bits [6]
      i. How many words are there in the address space.
      ii. How many words are there in the memory space.

6. Explain the following:
   (a) CPU - I O P Communication

(b) I O P

(c) IBM 370 I/O Channel. [5+5+6]

7. (a) What is pipelining? Explain. [8]

(b) Explain four segment pipelining. [8]

8. (a) Explain the working of 8 x 8 Omega Switching network.

(b) Explain the functioning of Binary Tree network with 2 x 2 Switches. Show a neat sketch. [8+8]

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Code No: R059210505 **Set No. 3**

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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Explain the terms compiler, linker, assembler, loader and describe how a C program or any other high level language program is executed in a system. Indicate entire process with a figure.
   (b) Distinguish between high level and low level languages?. What are the requirements for a good programming language? [16]
2. Explain about instruction, fetch, and decode cycles for a memory reference instruction. Draw a flow chart also to explain the same. Indicate clearly where and which processor registers comes into picture. Now let us assume while a instruction is in the middle of its decode cycle a interrupt is arrived. What is going to happen? Is the instruction is completed or not. If we want to stop there itself and handle the interrupt what are the difficulties? [16]
3. (a) What is a pipeline register. What is the use of it? Explain in detail. [8]
   (b) Why do we need some bits of current microinstruction to generate address of the next microinstruction. Support with a live example. [8]
4. (a) Draw a flow chart which explains multiplication of two signed magnitude fixed point numbers and give an example for the working of the method. [8]
   (b) Explain how we can identify arithmetic overflow is occurred while adding/subtracting two signed numbers. Draw the circuit for performing addition/subtraction of two 4 bit numbers that checks the over flow [8]
5. Explain the following Cache Mapping Techniques
   (a) Direct Mapping
   (b) Set Associative Mapping. [8+8]
6. (a) What is daisy chaining? Explain with neat sketch.
   (b) What is parallel priority interrupt method? Explain with neat sketch. [8+8]
7. Write short notes on the following:
   (a) RISC pipeline
   (b) Vector processing
   (c) Array processors. [5+5+6]

8. (a) Explain the working of 8 x 8 Omega Switching network.
   (b) Explain the functioning of Binary Tree network with 2 x 2 Switches. Show a neat sketch. [8+8]

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Code No: R059210505 **Set No. 4**

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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Give means to identify on whether or not has overflow has occurred in 2s complement addition or subtraction operations. Take one example for each possible situation and explain. Assume 4 bit registers. Let If overflow register E is also considered, check whether the result is corrector not [6]
   (b) Represent -32.75 and 18.125 in single precision IEEE 754 representation. [10]
2. Design register selection circuit to select one of the four 4-bit registers content on to bus. Give fuller explanation. [16]
3. (a) Explain nanoinstructions and nanometry. Why do we need them? [8]
   (b) Describe advantages and disadvantages of horizontal and vertical microcoded systems. [8]
4. (a) How many bits are needed to store the result addition, subtraction, multiplication and division of two n-bit unsigned numbers. Prove. [8]
   (b) What is overflow and underflow? What is the reason? If the computer is considered as infinite system do we still have these problems. [8]
5. Compare and contrast Asynchronous DRAM and Synchronous DRAM. [16]
6. (a) What is polling? Explain in detail.
   (b) What is daisy chaining? Explain. [8+8]
7. Explain the following with related to the Instruction Pipeline
   (a) Pipeline conflicts
   (b) Data dependency
   (c) Hardware interlocks
   (d) Operand forwarding
   (e) Delayed load
   (f) Pre-fetch target instruction
   (g) Branch target buffer
   (h) Delayed branch. [8×2=16]
8. (a) What is the functioning of cross bar switch network? Explain. With a neat sketch. [12]

(b) How many switch points are there in a cross bar switch network that connect 'p' Processors to 'm' Memory modules. [4]

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